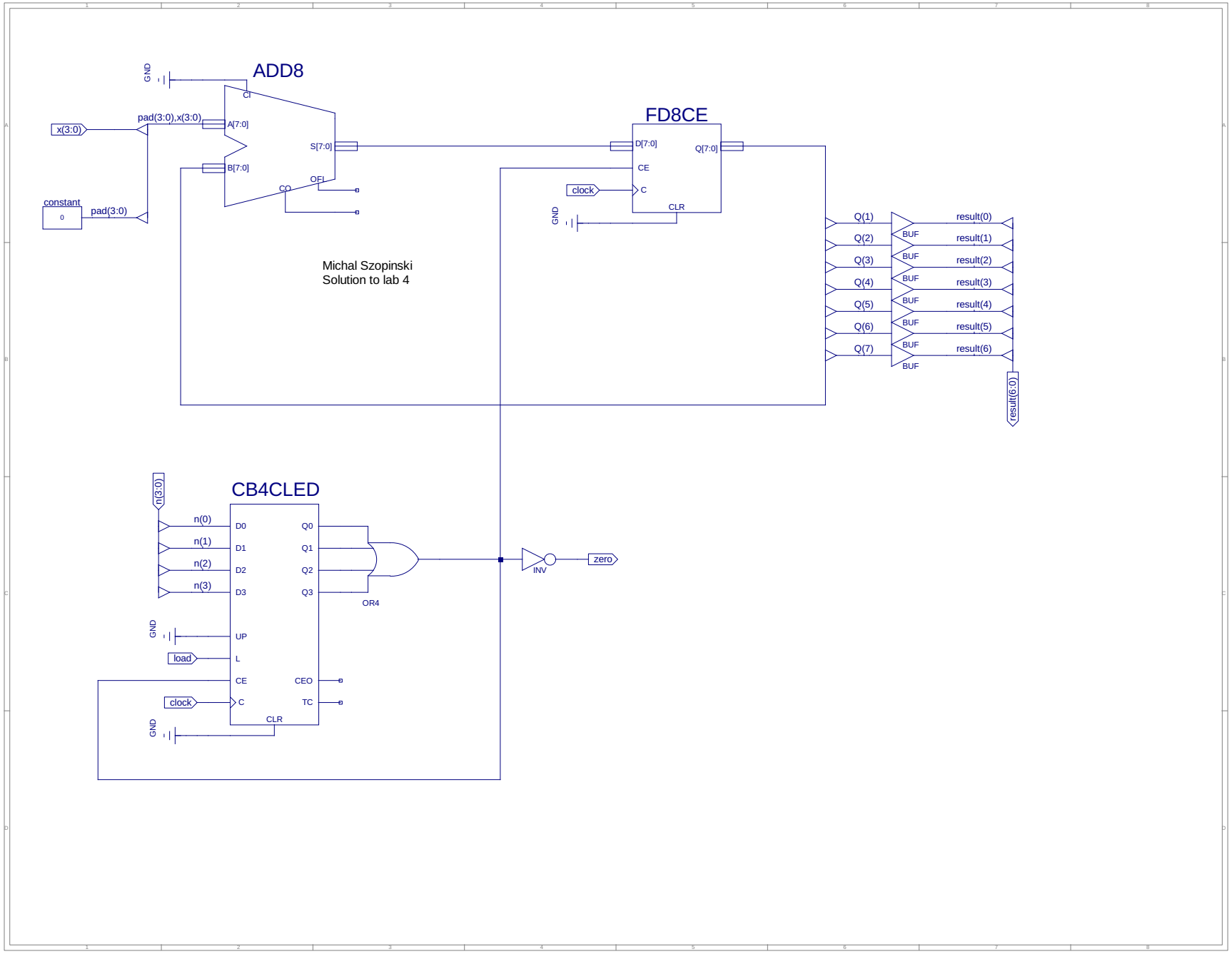
ADD8
GND
CI
x(3:0)
pad(3:0),x(3:0)
A[7:0]
B[7:0]
S[7:0]
CO
OFL
constant
0
pad(3:0)
FD8CE
D[7:0]
Q[7:0]
CE
clock
C
CLR
GND
Michal Szopinski
Solution to lab 4
Q(1)
Q(2)
Q(3)
Q(4)
Q(5)
Q(6)
Q(7)
BUF
result(0)
result(1)
result(2)
result(3)
result(4)
result(5)
result(6)
result(6:0)
CB4CLED
n(3:0)
n(0)
n(1)
n(2)
n(3)
D0
D1
D2
D3
Q0
Q1
Q2
Q3
OR4
INV
zero
GND
UP
load
L
CE
CEO
clock
C
TC
CLR
GND

```vhdl
-- Vhdl test bench created from schematic /home/mszopinski/Desktop/labko4/schem.sch - Sat Dec 14 00:00:52 2019
--
-- Notes:
-- 1) This testbench template has been automatically generated using types
-- std_logic and std_logic_vector for the ports of the unit under test.
-- Xilinx recommends that these types always be used for the top-level
-- I/O of a design in order to guarantee that the testbench will bind
-- correctly to the timing (post-route) simulation model.
-- 2) To use this template as your testbench, change the filename to any
-- name of your choice with the extension .vhd, and use the "Source->Add"
-- menu in Project Navigator to import the testbench. Then
-- edit the user defined section below, adding code to generate the
-- stimulus for your design.
--
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.ALL;
LIBRARY UNISIM;
USE UNISIM.Vcomponents.ALL;
ENTITY schem_schem_sch_tb IS
END schem_schem_sch_tb;
ARCHITECTURE behavioral OF schem_schem_sch_tb IS

   COMPONENT schem
   PORT( x  :   IN  STD_LOGIC_VECTOR (3 DOWNTO 0);
         clock :   IN  STD_LOGIC;
         load  :   IN  STD_LOGIC;
         zero  :   OUT STD_LOGIC;
         n :   IN  STD_LOGIC_VECTOR (3 DOWNTO 0);
         result    :   OUT STD_LOGIC_VECTOR (6 DOWNTO 0));
   END COMPONENT;

   SIGNAL result    :   STD_LOGIC_VECTOR (6 DOWNTO 0);
   SIGNAL x :   STD_LOGIC_VECTOR (3 DOWNTO 0) := "0000"; -- SET DEFAULT VALUES
   SIGNAL clock :   STD_LOGIC := '0';
   SIGNAL load  :   STD_LOGIC := '0';
   SIGNAL zero  :   STD_LOGIC;
   SIGNAL n :   STD_LOGIC_VECTOR (3 DOWNTO 0) := "0000";

BEGIN

   UUT: schem PORT MAP(
        x => x,
        clock => clock,
        load => load,
        n => n,
        result => result,
        zero => zero
   );

    clock <= not clock after 1 ns; -- SET CLOCK

-- *** Test Bench - User Defined Section ***
   tb : PROCESS
   BEGIN
      wait for 14 ns;

        x <= "0010";
        n <= "0011";
        load <= '1';
        wait for 2 ns;
        load <= '0';

        WAIT; -- will wait forever
   END PROCESS;
-- *** End Test Bench - User Defined Section ***

END;
```